Data Sheet No. PD-6.011B

INTERNATIONAL RECTIFIER IOR

HIGH VOLTAGE MOS GATE DRIVER

IR2110

General Description

The IR2110 is a high voltage, high speed MOS-gated power device driver with independent high side and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS outputs or with LSTTL outputs using pull-up resistors. Output drivers use low impedance totem-pole arrangement designed for low cross-conduction current spike. Propagation delays for the two channels are matched to simplify use in high frequency application. The floating channel can be used to drive a N-channel power MOSFET or IGBT in the high side configuration that operates off high voltage rail up to 500 volts.

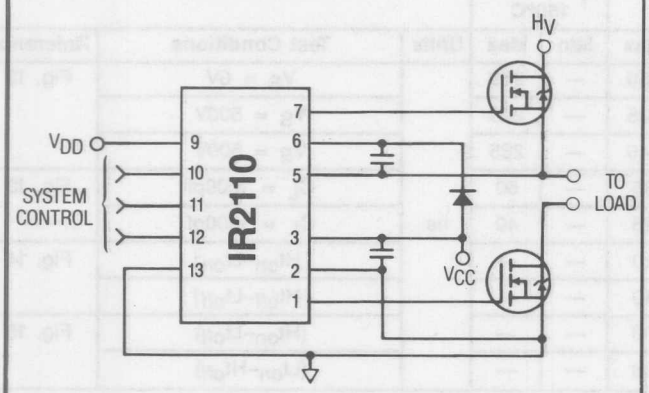
Applications

- High frequency switch-mode power supply
- DC and AC motor drives
- Electronic lamp ballast
- Battery charger
- Induction heating and welding
- Switching amplifier

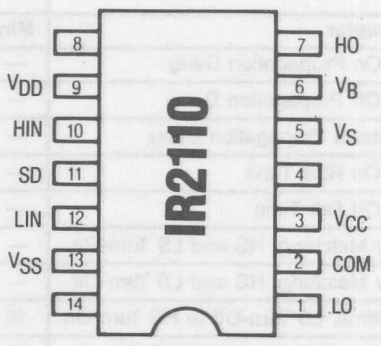
Features

- Floating supply designed for bootstrap operation
  - — Operating offset range from -4 to +500V
  - — dv/dt immunity rated at ±50V/ns
  - — Quiescent power dissipation of 1.6mW at 15V
- Wide output operating gate drive supply range from 10 to 20V
- Separate logic supply to interface with logic signal
  - — Operating supply range from 5 to 20V
  - — Logic and power ground operating offset range from –5 to +5V
- CMOS Schmitt-triggered inputs with hysteresis and pull-down
- Cycle by cycle edge-triggered shutdown logic
- Undervoltage lockout with hysteresis for both channels
- Output totem-pole driver designed to drive MOS-gated power devices
  - — Peak current capability at 2A minimum
  - — Switching time of 25ns typical into 1000pf load
- Matched propagation delay time for both channels
  - — Typical 120ns turn-on delay and 94ns turn-off delay
  - — Maximum rated matching differential of ±10ns
- Latch immune CMOS. Withstand >2A reverse current at I/O pins

Typical Connection



Pinout Assignment



For mechanical specifications see back page

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.
The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min	Max	Units
V_B	High Side Floating Supply Absolute Voltage	-0.5	V_S +20	V
V_S	High Side Floating Supply Offset Voltage	—	500	
V_{HO}	High Side Output Voltage	V_S -0.5	V_B +0.5	
V_{CC}	Low Side Fixed Supply Voltage	-0.5	20	
V_{LO}	Low Side Output Voltage	-0.5	V_{CC} +0.5	
V_{DD}	Logic Supply Voltage	-0.5	V_{SS} +20	
V_{SS}	Logic Supply Offset Voltage	V_{CC} - 20	V_{CC} +0.5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS} -0.5	V_{DD} +0.5	
dV_S/dt	Allowable Offset Supply Voltage Transient (Fig. 16)	—	50	V/ns
P_D	Package Power Dissipation @ T_A <= 25°C (Fig. 19)	—	1.6	W
R_{thJA}	Thermal Resistance, Junction to Ambient	—	75	°C/W
T_j	Junction Temperature	-55	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output Logic Timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions.
The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in Fig. 2 and 3.

Symbol	Parameter	Min	Max	Units
V_B	High Side Floating Supply Absolute Voltage	V_S +10	V_S +20	V
V_S	High Side Floating Supply Offset Voltage	-4	500	
V_{HO}	High Side Output Voltage	V_S	V_B	
V_{CC}	Low Side Fixed Supply Voltage	10	20	
V_{LO}	Low Side Output Voltage	0	V_{CC}	
V_{DD}	Logic Supply Vcltage	V_{SS} +5	V_{SS} +20	
V_{SS}	Logic Supply Offset Voltage	-5	5	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V and V_{SS} = COM unless otherwise specified.
The dynamic electrical characteristics are measured using the test circuit as shown in Fig. 11.

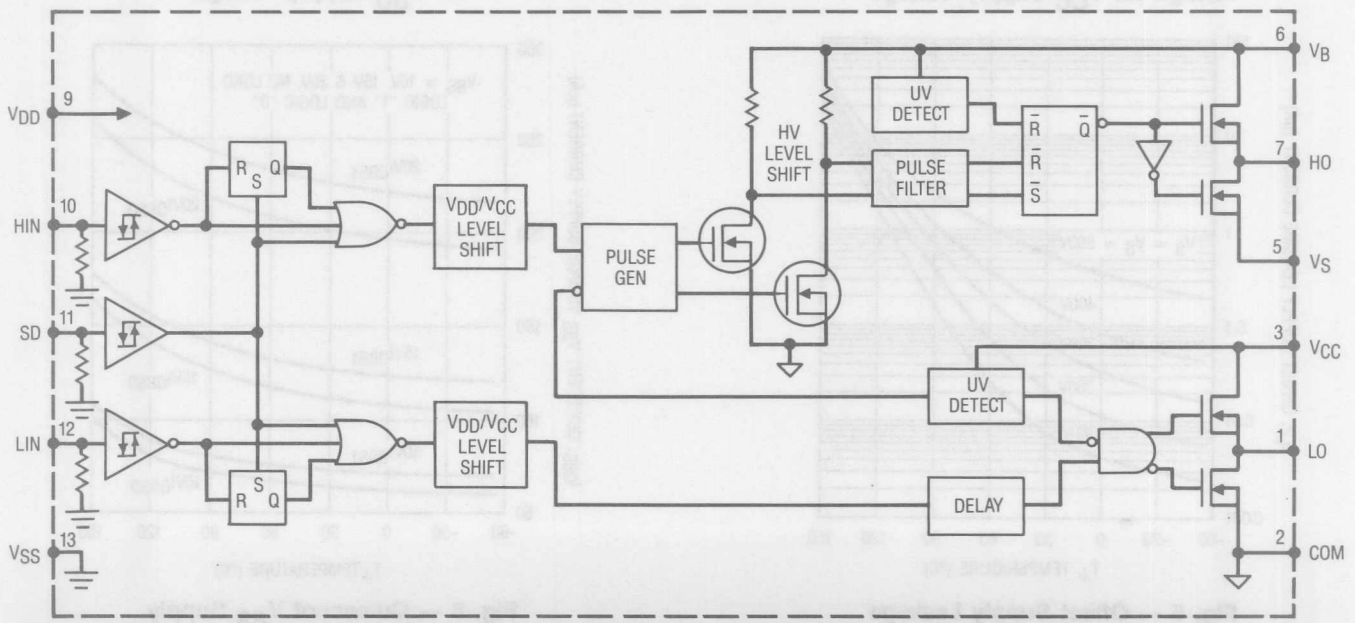
		T_j = 25°C			T_j = -55 to 150°C				
Symbol	Parameter	Min	Typ	Max	Min	Max	Units	Test Conditions	Reference
t_{on}	Turn-On Propagation Delay	—	120	150	—	260	ns	V_S = 0V	Fig. 12
t_{off}	Turn-Off Propagation Delay	—	94	125	—	220		V_S = 500V	
t_{sd}	Shutdown Propagation Delay	—	110	140	—	235		V_S = 500V	
t_r	Turn-On Rise Time	—	25	35	—	50		C_L = 1000pf	Fig. 13
t_f	Turn-Off Fall Time	—	17	25	—	40		C_L = 1000pf	
Mt_{on}	Delay Matching, HS and LS Turn-On	—	—	10	—	—		$\lvert Ht_{on}-Lt_{on}\rvert$	Fig. 14
Mt_{off}	Delay Matching, HS and LS Turn-Off	—	—	10	—	—		$\lvert Ht_{off}-Lt_{off}\rvert$	
DHt_{on}	Deadtime, LS Turn-Off to HS Turn-On	16	26	36	—	—		$(Ht_{on}-Lt_{off})$	Fig. 15
DLt_{on}	Deadtime, HS Turn-Off to LS Turn-On	16	26	36	—	—		$(Lt_{on}-Ht_{off})$	

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V unless otherwise specified.
The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic Input Pins: HIN, LIN and SD.
The VO and IO parameters are referenced to COM or V_S and are applicable to the respective Output Pins: HO or LO.

		T_j = 25°C			T_j = −55 to 150°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Units**	**Test Conditions**	**Reference**
V_{IH}	Logic "1" Input Voltage	3.1	—	—	3.3	—	V	V_{DD} = 5V	Fig. 4
		6.4	—	—	6.8	—		V_{DD} = 10V	
		9.5	—	—	10	—		V_{DD} = 15V	
		12.6	—	—	13.3	—		V_{DD} = 20V	
V_{IL}	Logic "0" Input Voltage	—	—	1.8	—	1.7		V_{DD} = 5V	
		—	—	3.8	—	3.6		V_{DD} = 10V	
		—	—	6	—	5.7		V_{DD} = 15V	
		—	—	8.3	—	7.9		V_{DD} = 20V	
V_{OH}	High Level Output Voltage, V_{BIAS}–VO	—	0.7	1.2	—	1.5	V	V_{IN} = V_{IH}, I_O = 0A	Fig. 10
V_{OL}	Low Level Output Voltage, VO	—	—	0.1	—	0.1		V_{IN} = V_{IL}, I_O = 0A	
I_{LK}	Offset Supply Leakage Current	—	—	50	—	250	μA	V_B = V_S = 500V	Fig. 5
I_{QBS}	Quiescent V_{BS} Supply Current	—	125	230	—	500		V_{IN} = V_{IH} or V_{IL}	Fig. 6
I_{QCC}	Quiescent V_{CC} Supply Current	—	180	340	—	600		V_{IN} = V_{IH} or V_{IL}	Fig. 7
I_{QDD}	Quiescent V_{DD} Supply Current	—	5	30	—	60		V_{IN} = V_{IH} or V_{IL}	
I_{IN+}	Logic "1" Input Bias Current	—	15	30	—	70		V_{IN} = 15V	Fig. 8
I_{IN-}	Logic "0" Input Bias Current	—	—	1	—	10		V_{IN} = 0V	
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	7.7	8.7	9.7	—	—	V		Fig. 9
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.3	8.3	9.3	—	—			
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	7.6	8.6	9.6	—	—			
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	7.2	8.2	9.2	—	—			
I_{O+}	Output High Short Circuit Pulsed Current	2	—	—	—	—	A	V_{OUT} = 0V, V_{IN} = 15V, PW <= 10 μs	
I_{O-}	Output Low Short Circuit Pulsed Current	2	—	—	—	—		V_{OUT} = 15V, V_{IN} = 0V, PW <= 10 μs	

Functional Block Diagram



Typical Performance Characteristics

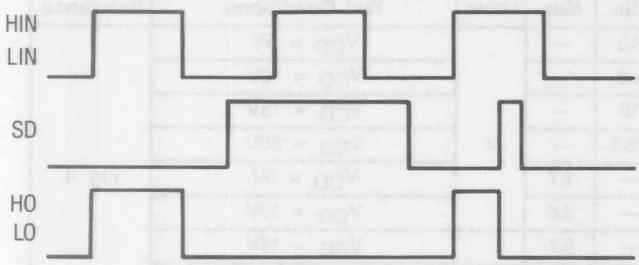


Fig. 1 — Input/Output Timing Diagram

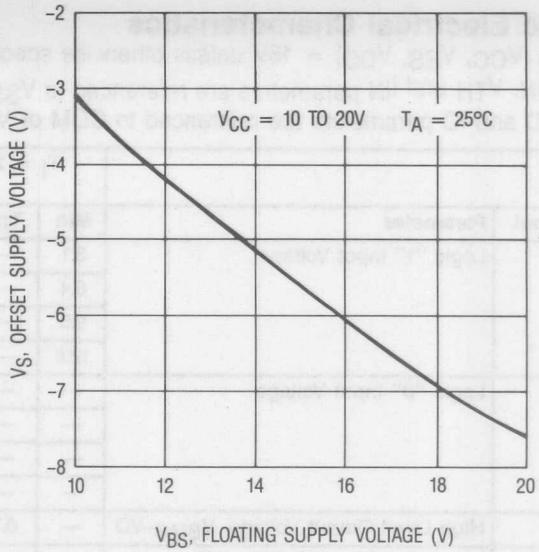


Fig. 2 — Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

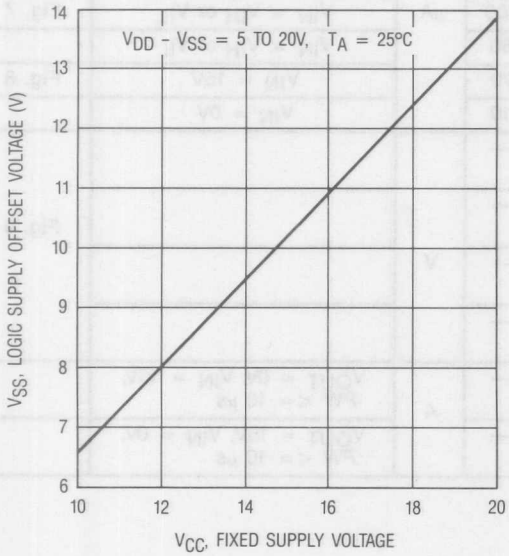


Fig. 3 — Maximum V_{SS} Positive Offset Voltage vs. V_{CC} Supply Voltage

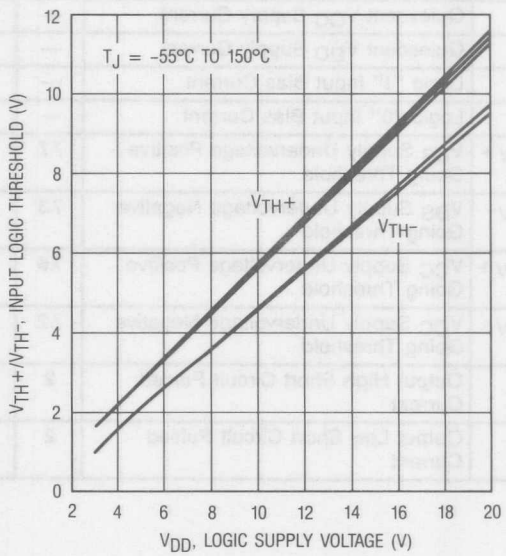


Fig. 4 — Input Logic Threshold vs. V_{DD} Supply Voltage

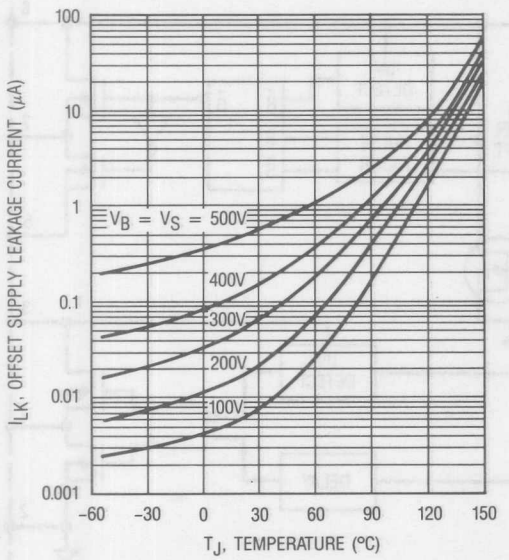


Fig. 5 — Offset Supply Leakage Current vs. Temperature

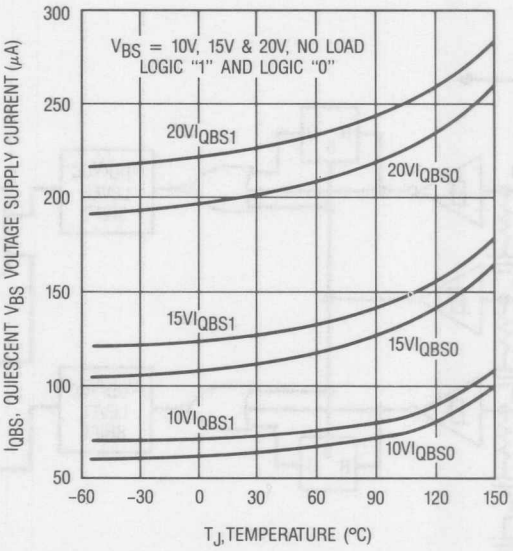


Fig. 6 — Quiescent V_{BS} Supply Current vs. Temperature

Typical Performance Characteristics

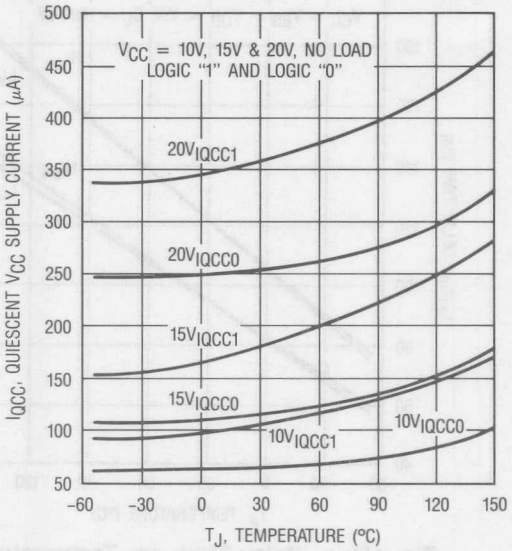


Fig. 7 — Quiescent V_{CC} Supply Current vs. Temperature

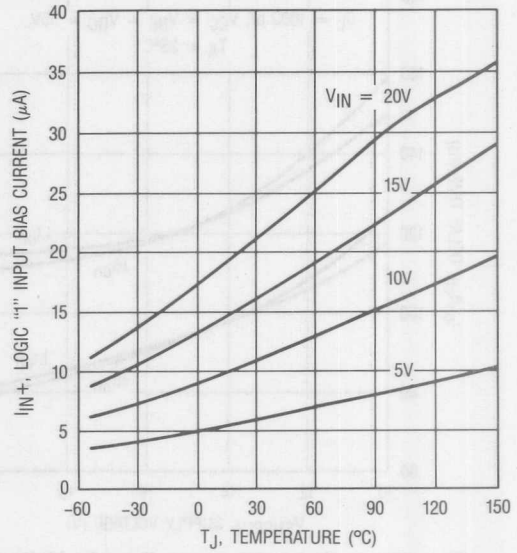


Fig. 8 — Logic "1" Input Bias Current vs. Temperature

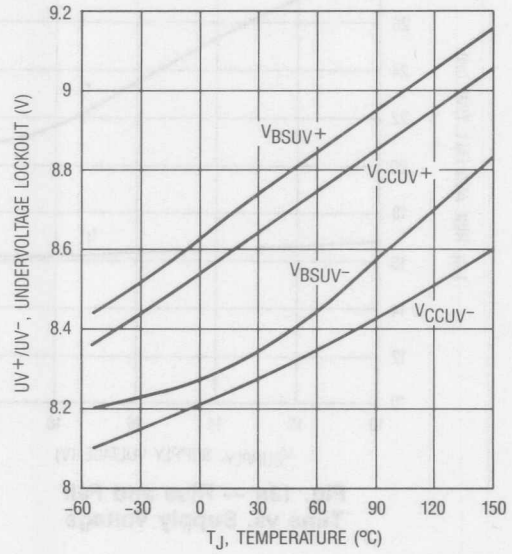


Fig. 9 — Undervoltage Lockout vs. Temperature

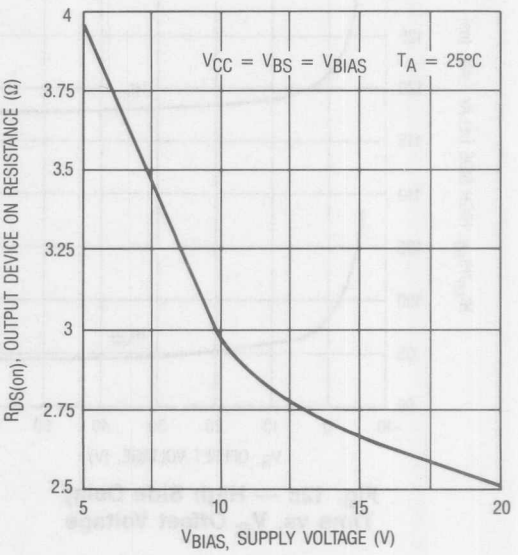


Fig. 10 — Output Device On Resistance vs. Supply Voltage

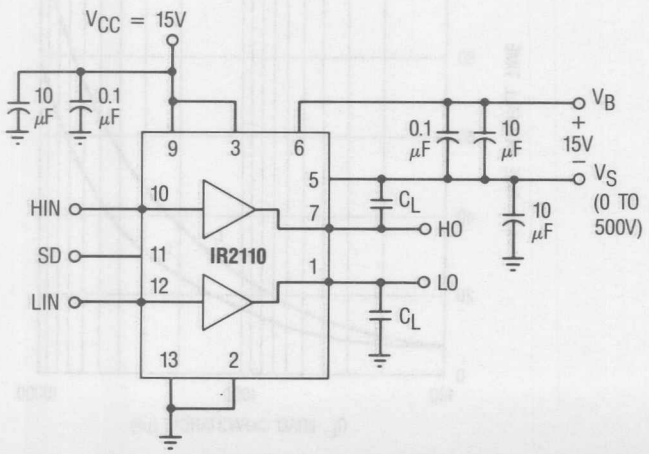


Fig. 11a — Switching Time Test Circuit

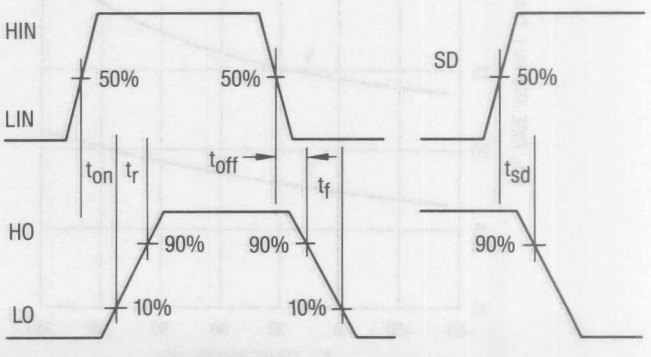


Fig. 11b — Switching Time Waveform Definition

Typical Performance Characteristics

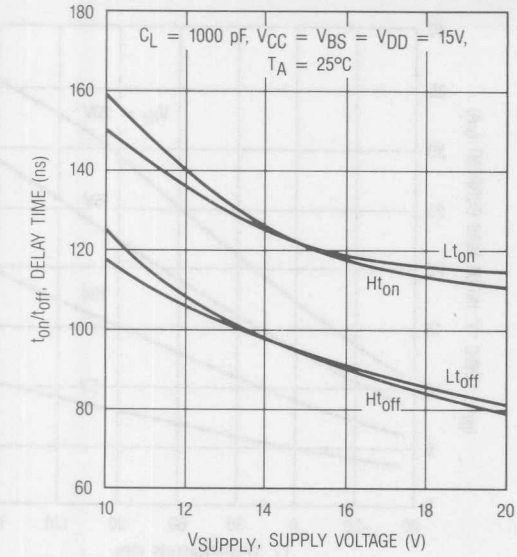


Fig. 12a — Delay Time vs. Supply Voltage

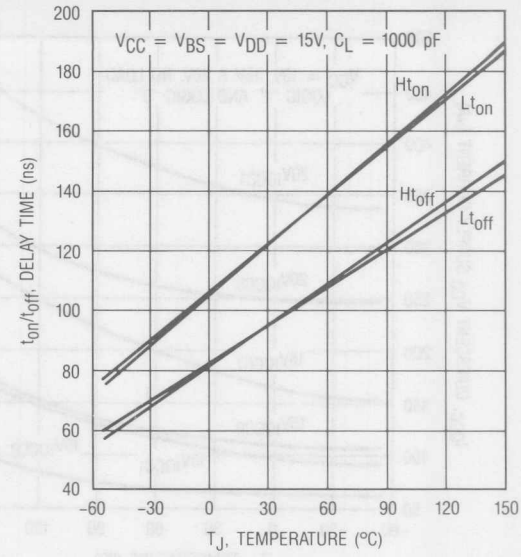


Fig. 12b — Delay Time vs. Temperature

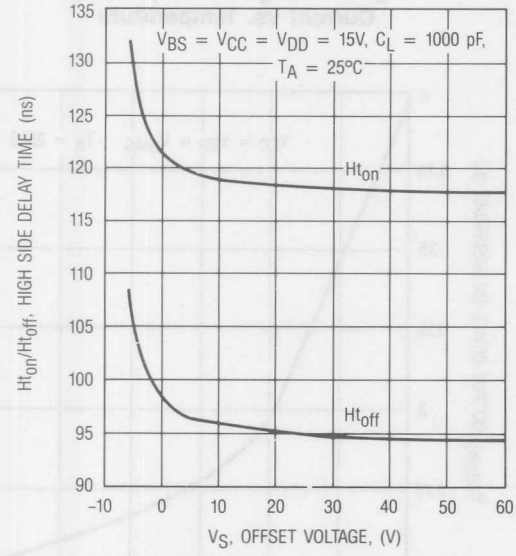


Fig. 12c — High Side Delay Time vs. V_S Offset Voltage

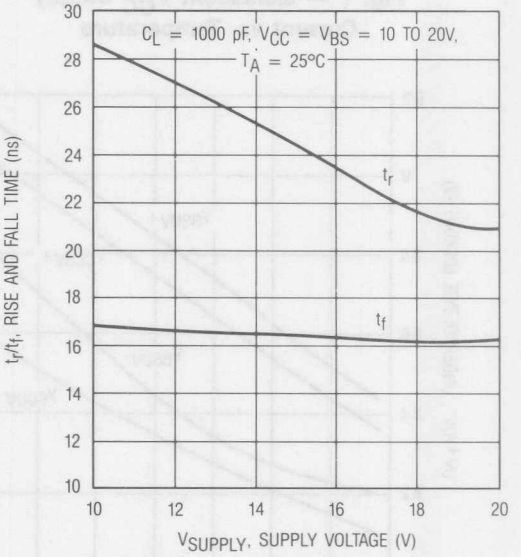


Fig. 13a — Rise and Fall Time vs. Supply Voltage

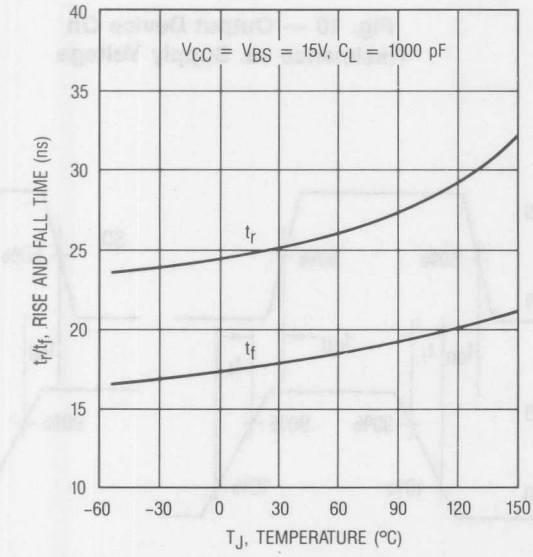


Fig. 13b — Rise and Fall Time vs. Temperature

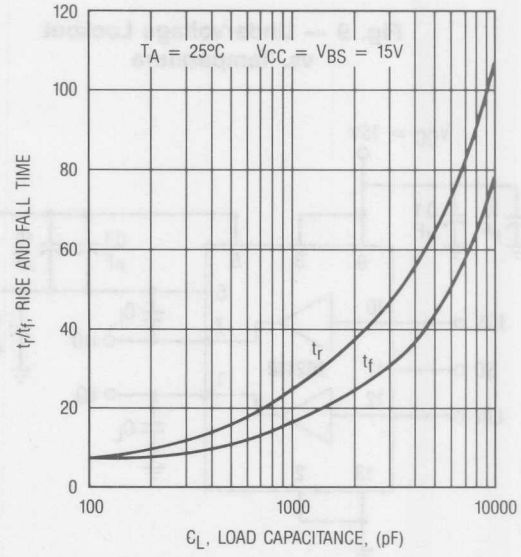
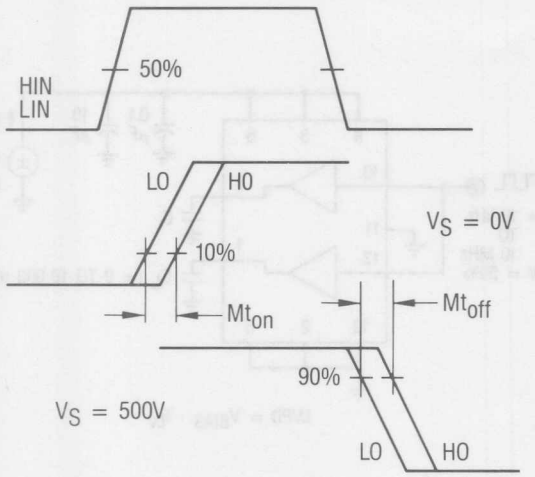


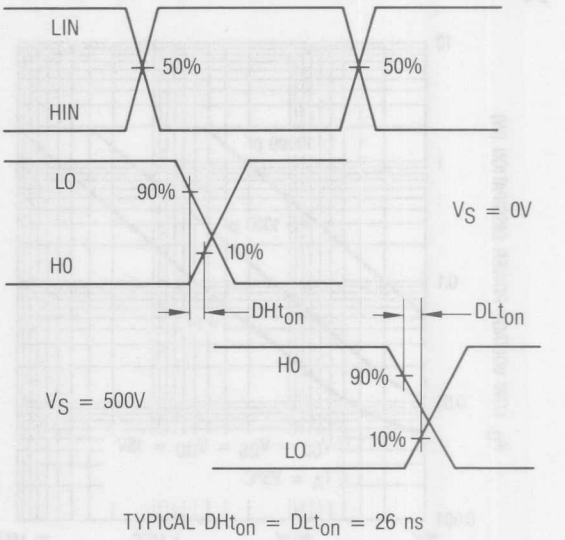
Fig. 13c — Rise Time/Fall Time vs. Load Capacitance

Typical Performance Characteristics



TYPICAL $Mt_{on} = Mt_{off}$ = 0 ns

Fig. 14 — Delay Matching Waveform Definitions



TYPICAL $DHt_{on} = DLt_{on}$ = 26 ns

Fig. 15 — Deadtime Waveform Definitions

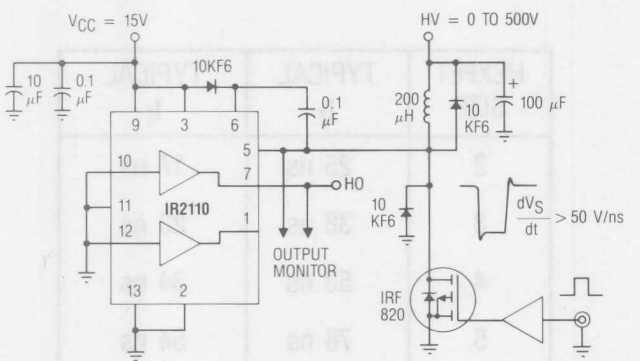


Fig. 16 — Floating Supply Voltage Transient Test Circuit

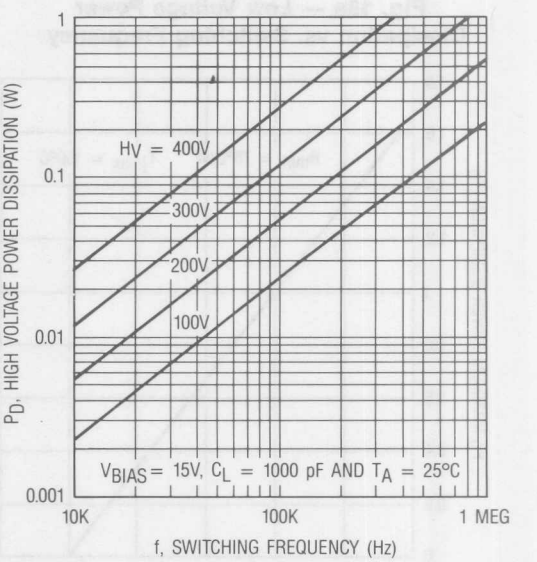


Fig. 17a — High Voltage Power Dissipation vs. Switching Frequency

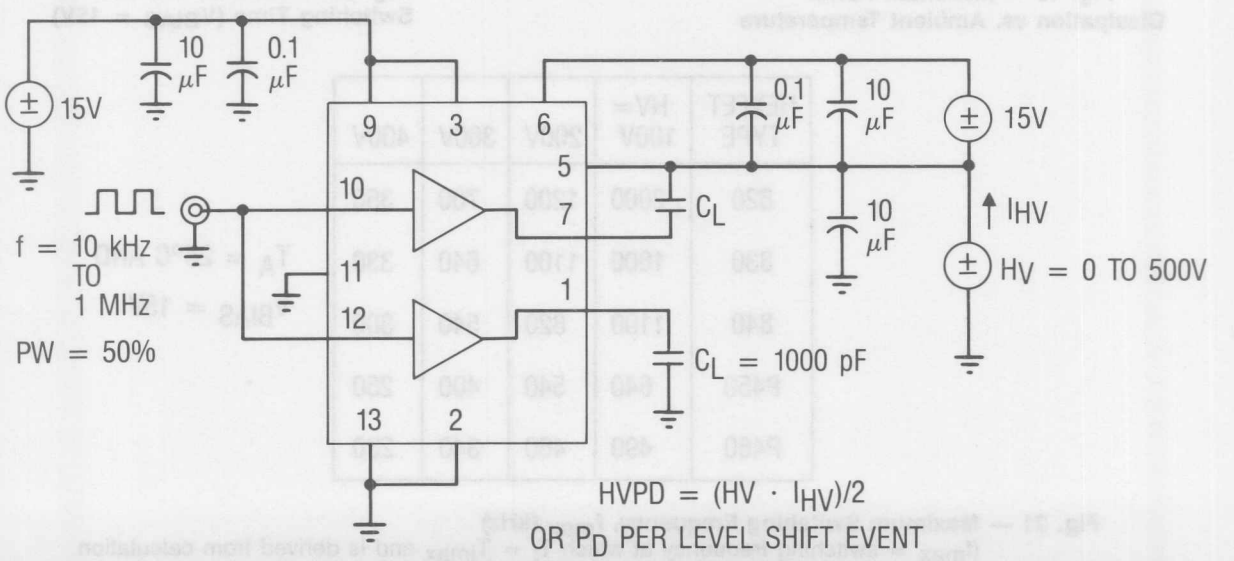


Fig. 17b — High Voltage Power Dissipation Test Circuit

Typical Performance Characteristics

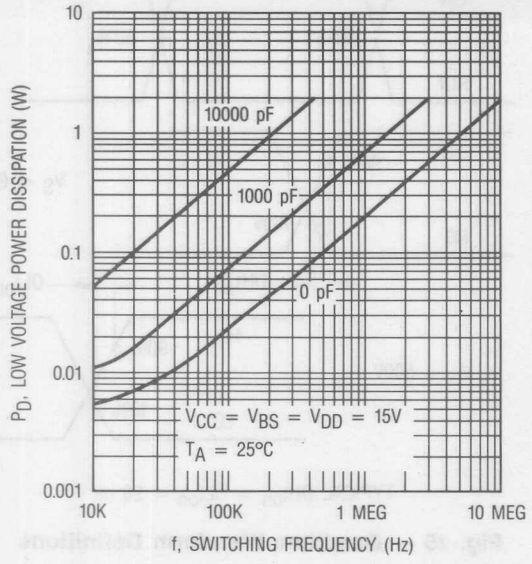


Fig. 18a — Low Voltage Power Dissipation vs. Switching Frequency

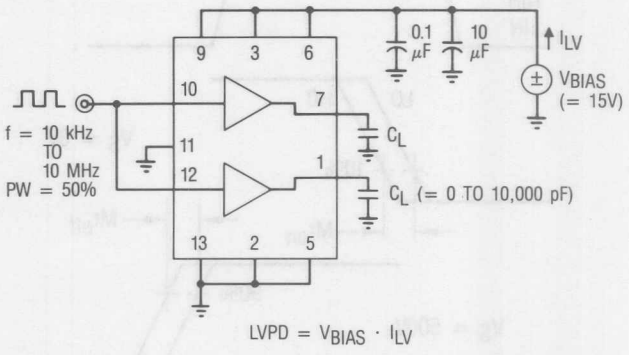


Fig. 18b. — Low Voltage Power Dissipation Test Circuit

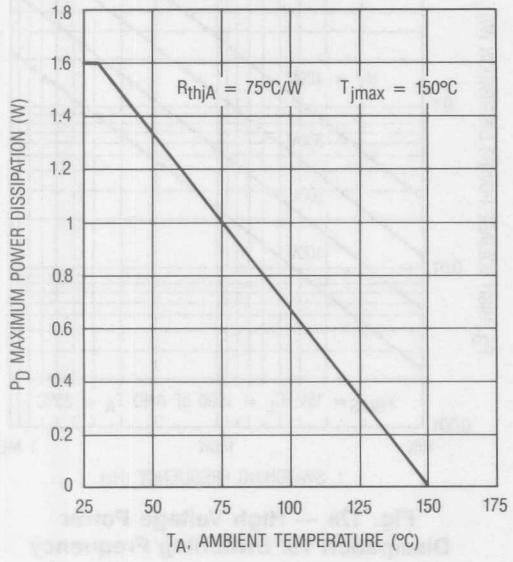


Fig. 19 — Maximum Power Dissipation vs. Ambient Temperature

HEXFET SIZE	TYPICAL t_r	TYPICAL t_f
2	25 ns	17 ns
3	38 ns	23 ns
4	53 ns	34 ns
5	78 ns	54 ns
6	116 ns	74 ns

Fig. 20 — HEXFET Die Size vs Switching Time (V_{BIAS} = 15V)

HEXFET TYPE	HV= 100V	200V	300V	400V
820	2000	1200	700	350
830	1600	1100	640	330
840	1100	820	540	300
P450	640	540	400	250
P460	490	460	340	230

T_A = 25°C AND V_{BIAS} = 15V

Fig. 21 — Maximum Switching Frequency, f_{max} (kHz)
(f_{max} = switching frequency at which T_j = T_{jmax} and is derived from calculation using typical electrical and thermal ratings. For operation at higher T_A, f_{max} should be derated accordingly.)

Functional Description

The IR2110 is a monolithic high voltage, high speed two channel power MOSFET or IGBT driver. Refer to the section on Functional Block Diagram for the internal partitioning of the various circuit blocks. The driver translates logic input signals into corresponding "in-phase" low impedance outputs. The low side channel output (LO) is referenced to a fixed rail (V_{CC}) and the high side channel output (HO) is referenced to a floating rail (V_{BS}) with offset capability up to 500V.

The logic circuit provides the control pulses for the two output channels corresponding to the logic inputs as indicated by the Input/Output Timing Diagram in Fig. 1. The HO and LO outputs are in phase with the HIN and LIN logic inputs. The two outputs will turn off when the SD input switches high and the outputs will remain off even after the SD input returns to low until the next rising edge of the respective inputs. In the case when V_{CC} is below the undervoltage trip point the UV detect circuit will send a shutdown signal to disable both channels. Also a separate UV detect block is used to disable the high side channel when V_{BS} is below its own undervoltage trip point. The logic inputs use Schmitt trigger circuits with a hysteretic band of $0.1 * V_{DD}$ to provide high noise immunity and can accept inputs with slow rise time. The logic circuit is referenced to its own logic supply to allow the use of a lower supply voltage than the output operating supply voltage. A high noise immunity V_{DD}/V_{CC} level-shifting circuit is used to translate logic signal to the output drivers. With a $\pm$5V rated offset capability between the logic ground (V_{SS}) and power ground (COM), the logic circuit is unaffected by the noise coupling generated by the switching action of the output drivers.

Propagation delay for the two channels are matched using the low side delay circuit to simplify the timing requirements of the control pulses. The turn-on delay is matched at 120ns for the low side channel (Lt_{on}) and the high side channel (Ht_{on}) with V_S at 0V since the high side turn-on command is usually executed when V_S is at or near 0V. The turn-off delay is matched at 94ns for the low side channel (Lt_{off}) and the high side channel (Ht_{off}) with V_S at 500V since the high side turn-off command is usually executed after the high side power MOSFET is "on" and V_S is at or near the high voltage rail.

Both channels use identical low cross-conduction totem pole output connected transistors. The output driver consists of two N-channel MOSFETs with peak current capability above 2A and on resistance of less than 3 ohms (Fig. 10). One output MOSFET is connected as a source follower and the other in common source configuration. Because of the totem pole arrangement the rise time is slower than the fall time driving capacitive load. For a typical 3300pf load the rise and fall times are 50ns and 33ns respectively.

For the high side channel, narrow "On" and "Off" pulses triggered respectively by the rising and the falling edge of HIN are generated by the pulse generator. The respective pulses are used to drive separate high voltage DMOS level translators that set or reset a RS latch operating off the floating rail. Level shifting of the ground referenced HIN signal is thus accomplished by transposing the signal references to the floating rail. Because each high voltage DMOS level translator is turned on for only the duration of the short "On" or "Off" pulses with each set or reset event, power dissipation is minimized. False triggering of the RS latch from fast dv/dt transients on the V_S node is effectively differentiated from normal pull-down pulses through a pulse discriminator circuit such that the high side channel is essentially immune to any magnitude of dv/dt value. Also the high voltage level shifting circuit is designed to function normally even when the V_S node swings more than 4V below the COM pin. This condition can often occur during the recirculation period of the output free-wheeling diode.

Application Guidelines

(Also see Application Note AN-978A for details)

The IR2110 is typically used to drive two high voltage N-channel power MOSFETs or IGBTs configured in half-bridge, dual-forward or other topologies. The fixed rail referenced output is used to drive a low side connected power MOSFET. The floating output channel is used to drive a power MOSFET in the high side configuration that requires an over-rail gate drive. Refer to the section on Typical Applications for the various circuit topologies where the IR2110 is applicable.

Typically, the floating supply is derived from the fixed supply using a bootstrap technique as shown in the section on Typical Connection. The charging diode must have a voltage withstand capability higher than the peak HV bus voltage. To minimize power dissipation a fast recovery diode is recommended. The value of the bootstrap capacitor depends on the switching frequency, duty cycle and gate charge requirement of the power MOSFET. The voltage across the capacitor should not be allowed to drop below the under-voltage lockout threshold, otherwise protective shutdown will occur. A 0.1 μF capacitor is usually suitable for applications switching above 5 KHz.

Supply bypass capacitors between V_{CC} and COM and between V_{DD} and V_{SS} are required to supply the transient current needed for switching the capacitive loads. These capacitors, together with the reservoir capacitor across V_B and V_S, must be connected close to the device. A 0.1 μF ceramic disk capacitor in parallel with a 1 μF tantalum capacitor is recommended for V_{CC} bypass. A 0.1 μF ceramic disk capacitor is usually adequate for the logic supply.

The outputs of the IR2110 are designed to deliver gate drives for fast switching speed even for high current power MOSFETs with relatively high gate charge requirement. The typical switching speed for various standard power MOSFET sizes is shown in Fig. 20. To minimize inductance in the gate drive loop, each MOSFET should have its own dedicated connection going to Pin 2 and 5 of the IR2110 for the return of the gate drive signal. For smaller power MOSFETs a series gate resistor for each output is recommended to limit switching speed. The value of the gate resistor depends on EMI requirement, switching losses and the maximum allowable dv/dt.

The total power dissipation of the IR2110 is a function of HV bus voltage, V_{CC} and V_{DD} voltages, switching frequency, duty cycle, delivered gate drives charge, and operating junction temperature. The total dissipation can be divided into two categories: High voltage and low voltage switching.

The high voltage dissipation can be calculated by the following formula:

$$PD(HV) = \underbrace{HV * I_{LK} * d}_{\text{static}} + \underbrace{(V_{Bon} + V_{Boff}) * Qp * f}_{\text{dynamic}}$$

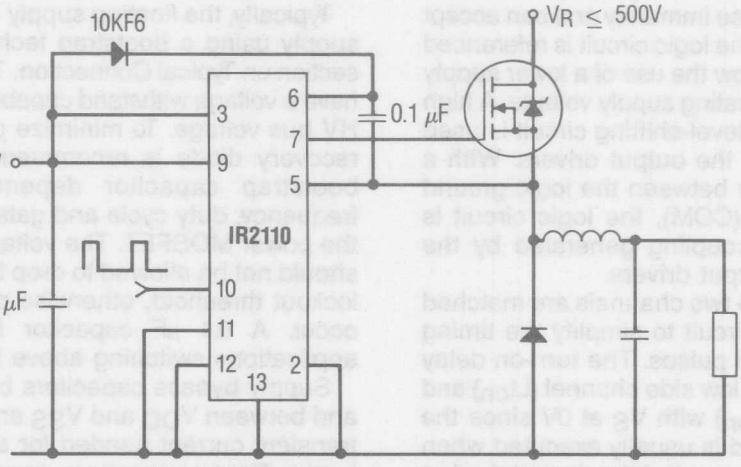
with HV the high voltage bus voltage, I_{LK} the leakage current of V_B to ground, d the duty cycle of the high side switch, Qp the pulsed charge of high voltage level shifter, V_{Bon} the average voltage of V_B during the turn-on pulse, V_{Boff} the average voltage of V_B during the turn-off pulse and f the switching frequency of the high side channel. The level shifting losses are usually much larger than the leakage losses such that the static term can be neglected for most applications. Fig. 17 shows the total high voltage dissipation as a function of switching frequency at various fixed V_S voltage level. Note that the graph only shows the high voltage power dissipation per set or reset event at the particular fixed V_S level. Keep in mind that in actual application V_S is swinging during the level shifting event.

The low voltage dissipation can be calculated by the following formula:

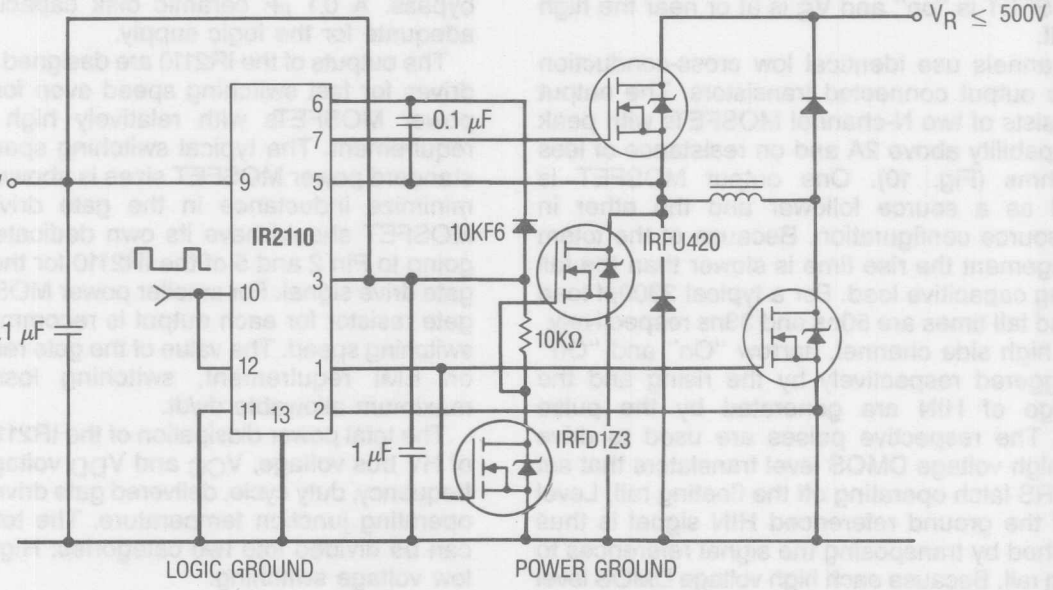
$$PD(LV) = \underbrace{V_{bias} * IQ_{tot}}_{\text{static}} + \underbrace{2 * V_{bias} * Qg * f + V_{bias} * Q_{cmos} * f}_{\text{dynamic}}$$

with V_{bias} the low voltage bias voltage assuming $V_{DD} = V_{CC} = V_{BS}$, IQ_{tot} the total quiescent current, Qg the delivered gate charge per driven MOSFET, f the switching frequency and Q_{cmos} the switching losses associated with the internal CMOS circuitry. The quiescent losses are usually much smaller than the dynamic losses such that the static term can be neglected. Fig. 18 shows the total low voltage power dissipation as a function of switching frequency at various load conditions. The switching losses associated with internal circuitry (Q_{cmos}) are shown in the graph for the case of "0 pf" loading condition.

Typical Applications

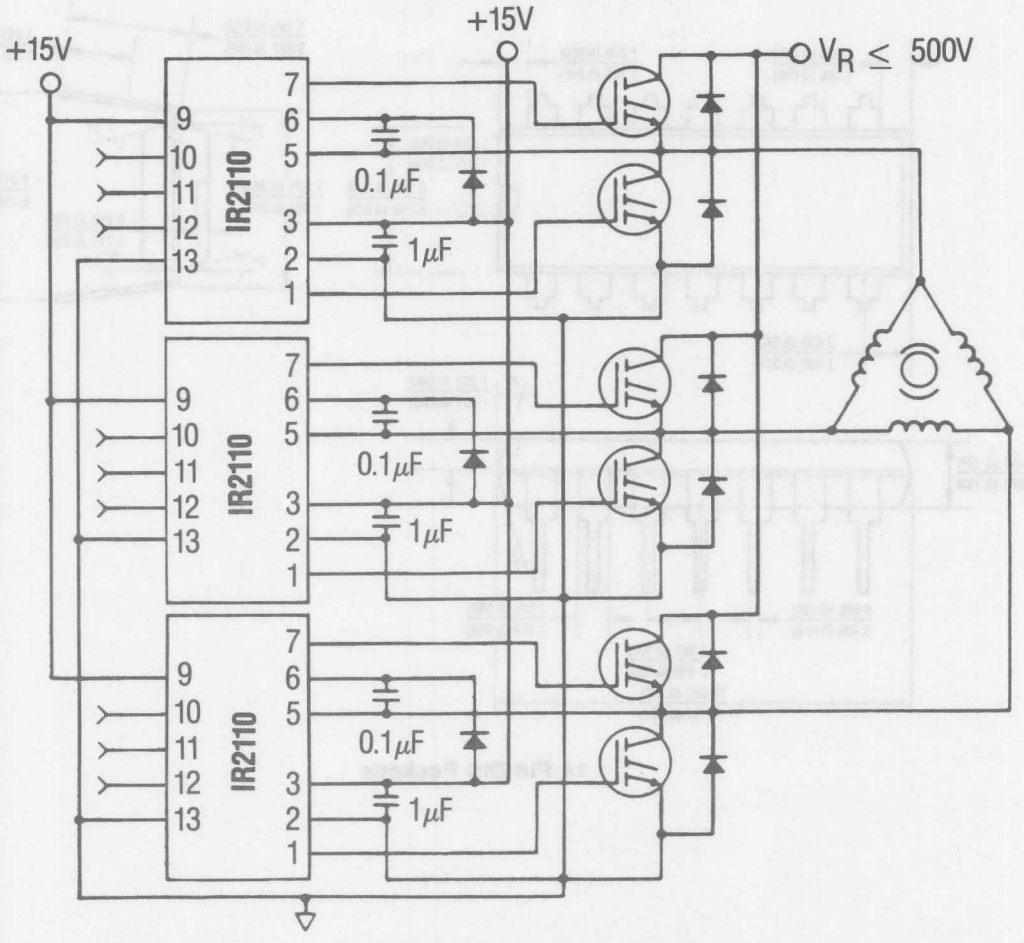


Buck Converter

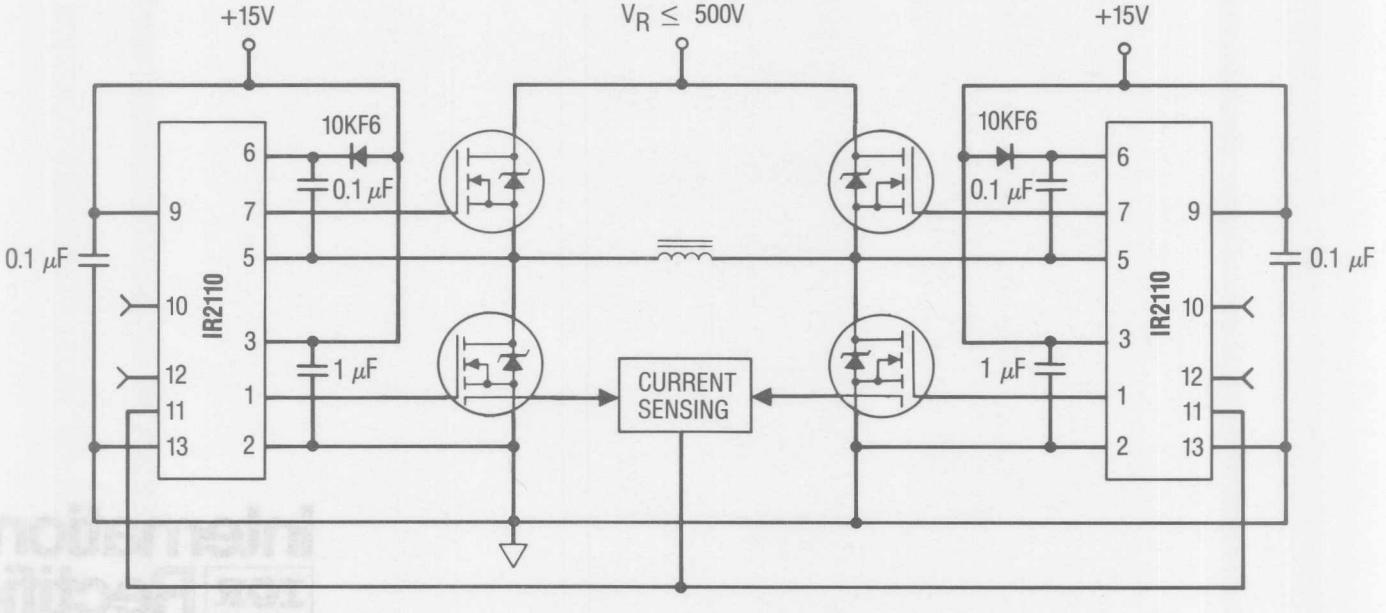


Dual Forward Converter

Typical Applications Continued



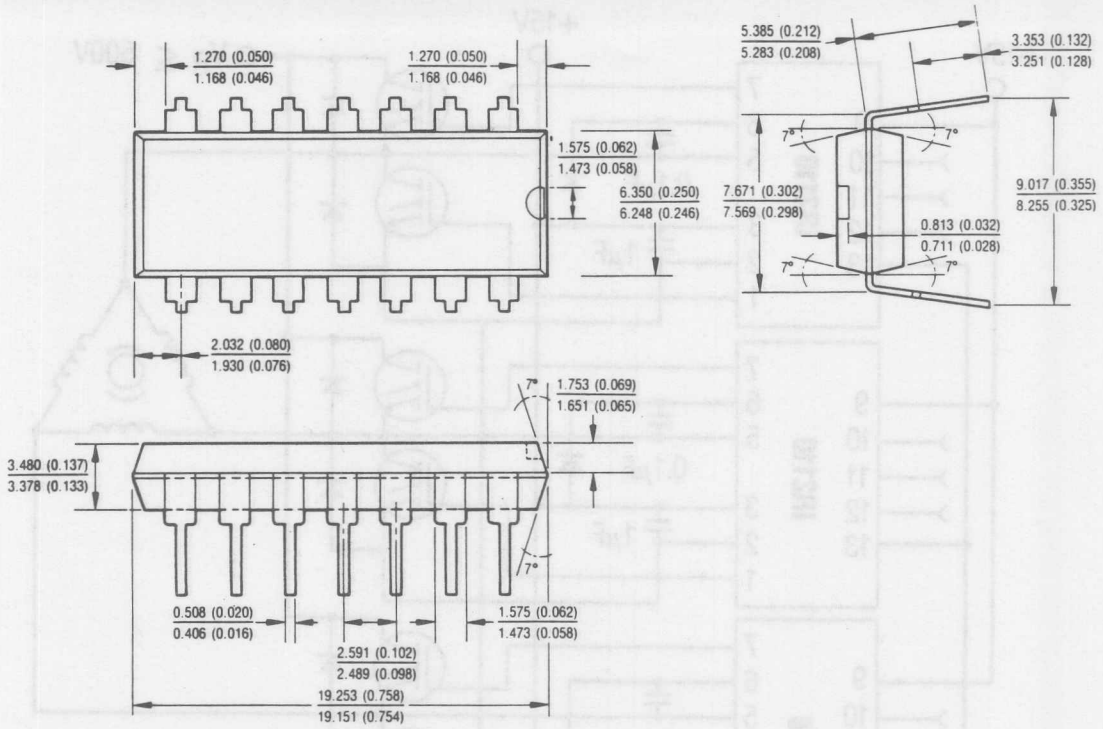
3-Phase Bridge Motor Drive



H-Bridge

Typical implementation of an H-bridge with cycle-by-cycle current mode control

Mechanical Specification



14 Pin Dip Package

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (213) 772-2000, Twx: 4720403
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB England, Tel: (0883) 713215, Twx: 95219

IR CANADA: 101 Bentley St., Markham, Ontario L3R 3L1. Tel: (416) 475-1897. **IR GERMANY:** Saalburgstrasse 157, D-6380 Bad Homburg, Tel: 6172-37066. **IR ITALY:** Via Liguria 49 10071 Borgaro, Torino, Tel: (011) 470 1484. **IR FAR EAST:** K&H Building, 30-4 Nishiikebukuro 3-Chrome, Toshima-ku, Tokyo 171 Japan, Tel: (03) 983 0641. **IR SOUTHEAST ASIA:** 190 Middle Road, HEX 10-01 Fortune Centre, Singapore 0718, Tel: (65) 336 3922.

Sales Offices, Agents and Distributors in Major Cities Throughout the World.

Printed in the USA 12/90

Data Sheet No. PD-6.016

INTERNATIONAL RECTIFIER IOR

HIGH VOLTAGE MOS GATE DRIVER

IR2110S

General Description

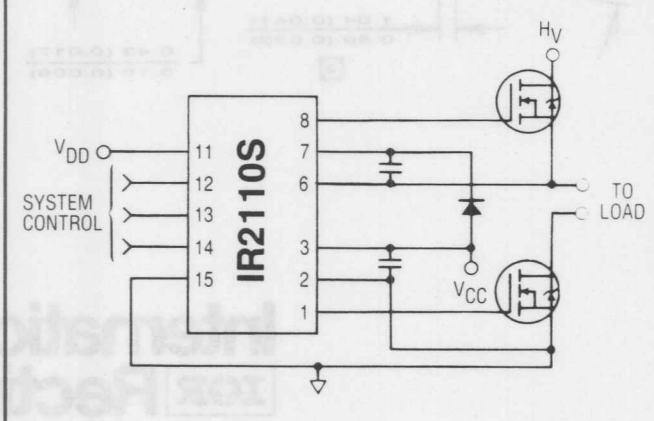
The IR2110S is the SOIC or small outline IC form of the IR2110; a high voltage, high speed MOS-gated power device driver with independent high side and low side referenced channels. Refer to **Data Sheet No. PD-6.011B** for electrical parameters. This surface mounted device is particularly well suited for applications that require high density circuit layout.

With the exception of the maximum thermal resistance and maximum power dissipation all of the device characteristics specified on the IR2110 plastic dip package apply to the IR2110S. As with the IR2110 plastic dip the IR2110S has a maximum operating temperature range from –55°C to 150°C.

Absolute Maximum Ratings

Symbol	Parameter	Max	Units
P_D	Package Power Dissipation @ Ta < = 25C, Fig. 1	1.25	W
R_{thJa}	Thermal Resistance, Junction to Ambient	100	°C/W

Typical Connection



Pinout Assignment

FOR MECHANICAL SPECIFICATIONS SEE BACK PAGE

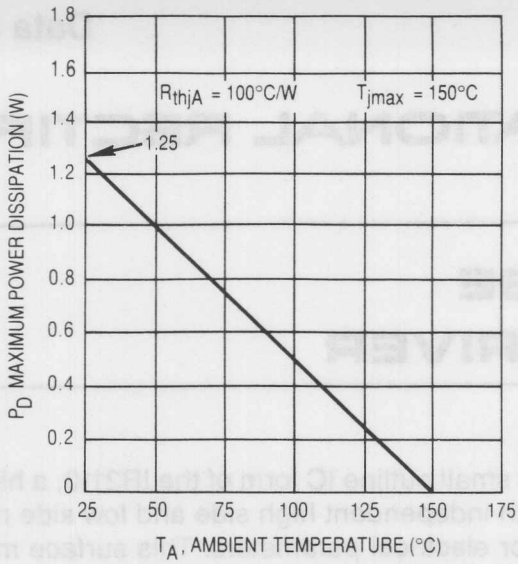


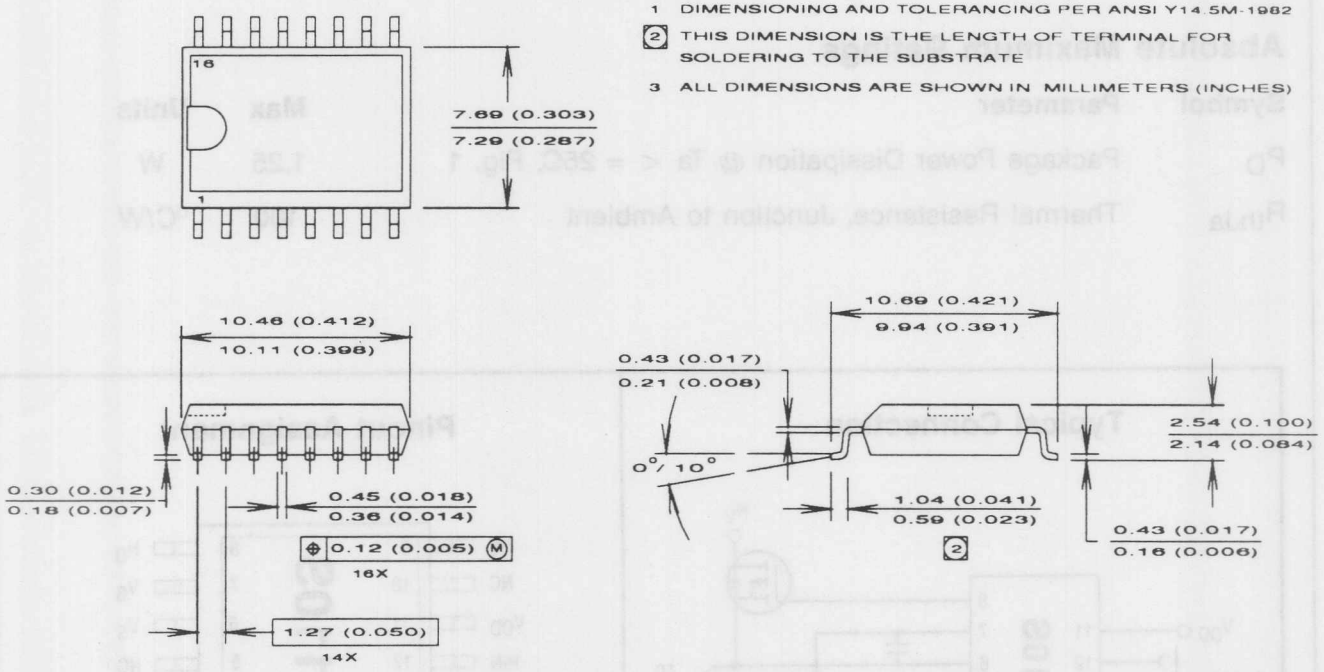
Fig. 1 – Maximum Power Dissipation vs. Ambient Temperature

NOTES:

1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982

2 THIS DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO THE SUBSTRATE

3 ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)



WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (213) 772-2000, Twx: 4720403
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB England, Tel: (0883) 713215, Twx: 95219

IR CANADA: 101 Bentley St., Markham, Ontario L3R 3L1. Tel: (416) 475-1897. **IR GERMANY:** Saalburgstrasse 157, D-6380 Bad Homburg, Tel: 6172-37066. **IR ITALY:** Via Liguria 49 10071 Borgaro, Torino, Tel: (011) 470 1484. **IR FAR EAST:** K&H Building, 30-4 Nishiikebukuro 3-Chrome, Toshima-ku, Tokyo 171 Japan, Tel: (03) 983 0641. **IR SOUTHEAST ASIA:** 190 Middle Road, HEX 10-01 Fortune Centre, Singapore 0718, Tel: (65) 336 3922.

Sales Offices, Agents and Distributors in Major Cities Throughout the World.

Printed in the USA 8/90

Data Sheet No. PD-6.014

INTERNATIONAL RECTIFIER IOR

HIGH VOLTAGE MOS GATE DRIVER

IR2110C

General Description

The IR2110C is the die form of the IR2110 (refer to **Data Sheet No. PD-6.011B**); a high voltage, high speed MOS-gated power device driver with independent high side and low side referenced channels. The IR2110C is ideal for use in power hybrid modules where substantial savings in weight and volume can be obtained.

Some of the device characteristics specified on the packaged device are packaging dependent and therefore limits cannot be guaranteed in die form. These are:

Maximum power dissipation	P_D max.
Maximum thermal resistance	R_{thJA} max.
Minimum short circuit current	$I_O \pm$ min.

and dynamic electrical characteristics

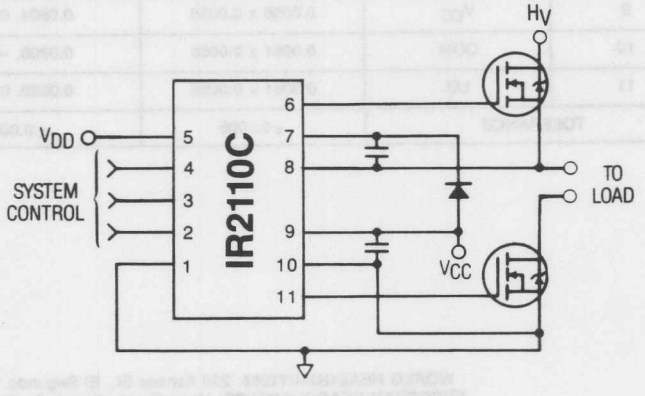
Maximum propagation delays
Maximum rise and fall times
Maximum delay matching
Maximum and minimum deadtimes.

All typical performance characteristics of the IR2110 apply to the IR2110C, however, final package performance is dependent upon the user's assembly techniques.

Mechanical Specifications

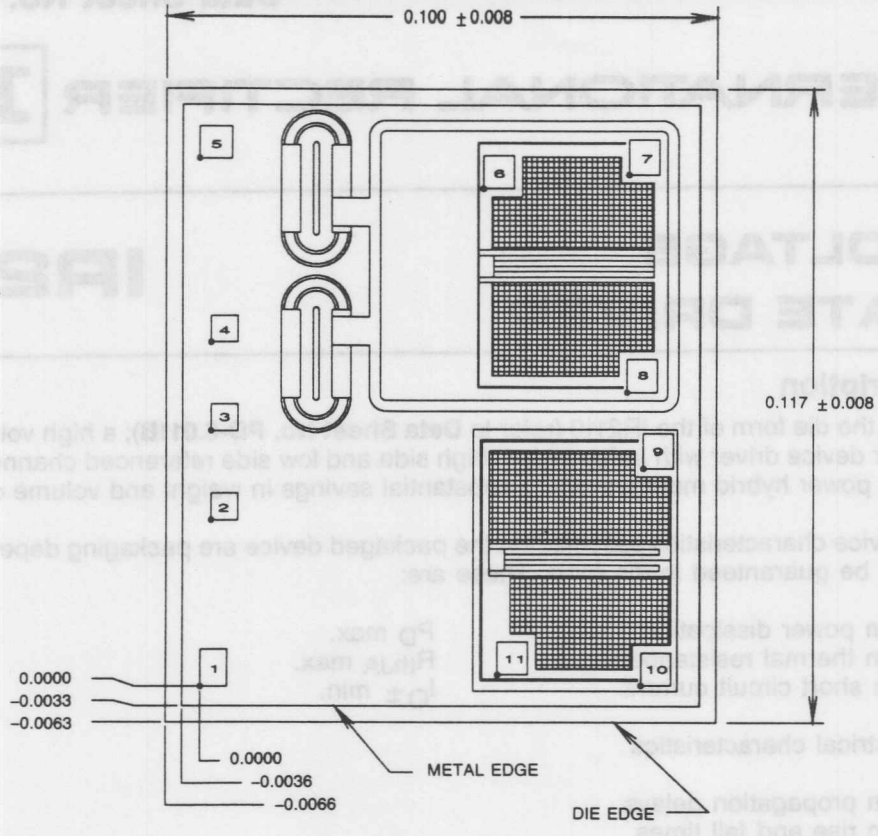
Front Metal	aluminum 1% silicon
Back Metal	chromium-nickel-silver
Die Thickness	16 ± 1 mils

Typical Connection



Die Connection — Refer to Diagram on Reverse Side

BRIDGE DRIVER



LEGEND

DIMENSIONS IN INCHES

PAD #	FUNCTION	DIMENSIONS H x W	DATUM X Y
1	V_{SS}	0.0069 x 0.0049	0.0000, 0.0000
2	LIN	0.0049 x 0.0049	0.0019, 0.0307
3	SD	0.0049 x 0.0049	0.0019, 0.0471
4	HIN	0.0049 x 0.0049	0.0019, 0.0635
5	V_{DD}	0.0059 x 0.0059	–0.0002, 0.0975
6	HO	0.0061 x 0.0055	0.0513, 0.0920
7	V_B	0.0065 x 0.0055	0.0778, 0.0946
8	V_S	0.0061 x 0.0055	0.0774, 0.0542
9	V_{CC}	0.0065 x 0.0055	0.0804, 0.0402
10	COM	0.0061 x 0.0055	0.0800, –0.0002
11	LO	0.0061 x 0.0055	0.0539, 0.0022
TOLERANCE		±0.0005	±0.0002

International
IOR Rectifier

WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (213) 772-2000, Twx: 4720403
EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB England, Tel: (0883) 713215, Twx: 95219

IR CANADA: 101 Bentley St., Markham, Ontario L3R 3L1. Tel: (416) 475-1897. **IR GERMANY:** Saalburgstrasse 157, D-6380 Bad Homburg, Tel: 6172-37066. **IR ITALY:** Via Liguria 49 10071 Borgaro, Torino, Tel: (011) 470 1484. **IR FAR EAST:** K&H Building, 30-4 Nishiikebukuro 3-Chrome, Toshima-ku, Tokyo 171 Japan, Tel: (03) 983 0641. **IR SOUTHEAST ASIA:** 190 Middle Road, HEX 10-01 Fortune Centre, Singapore 0718, Tel: (65) 336 3922.

Sales Offices, Agents and Distributors in Major Cities Throughout the World.

Printed in the USA 4/90